WHAT IS CLAIMED IS:

1. A method of manufacturing a semiconductor device, comprising:

forming a gate structure over a substrate;

forming an interconnect layer over the gate structure and the substrate;

forming a cap layer over the interconnect layer;

planarizing the interconnect layer and the cap layer to form a substantially planar surface, the substantially planar surface having a portion of exposed interconnect layer and a portion of exposed cap layer;

forming a mask layer over the exposed portion of the planarized interconnect layer; and

removing material underlying the exposed portion of the planarized cap layer.

2. The method of Claim 1 wherein the interconnect layer is formed over the gate structure to a thickness that is less than a height of the gate structure.

3. The method of Claim 1 wherein the mask layer is formed by an anneal process.

4. The method of Claim 1 further comprising removing the mask layer after removing the planarized cap layer.

5. The method of Claim 1 wherein a first removal rate of the interconnect layer during the planarizing is greater than a second removal rate of the cap layer during the planarizing.

6. The method of Claim 5 wherein the first removal rate is at least three times greater than the second removal rate.

7. The method of Claim 1 wherein the cap layer is formed directly on the interconnect layer.

8. The method of Claim 1 wherein a portion of the cap layer is separated from the substrate by a distance that is less than the height of the gate structure.

9. The method of Claim 1 wherein the cap layer comprises SiO_2.

10. The method of Claim 1 wherein the cap layer comprises Si_3N_4.

11. The method of Claim 10 wherein the mask layer comprises SiO_2.

12. The method of Claim 1 wherein removing material includes removing the cap layer and removing polysilicon.

13. The method of Claim 1 wherein the cap layer has a thickness ranging between 100 angstroms and 2000 angstroms before planarizing.

14. The method of Claim 1 wherein the planarizing includes chemical-mechanical polishing (CMP).

15. The method of Claim 14 wherein the CMP includes planarizing the cap layer and the interconnect layer between a rotatable polishing head and a rotatable polishing platen at a polishing head speed ranging between 75 rpm and 200 rpm.

16. The method of Claim 14 wherein the CMP includes planarizing the cap layer and the interconnect layer between a rotatable polishing head and a rotatable polishing platen at a platen speed ranging between 65 rpm and 150 rpm.

17. The method of Claim 14 wherein the CMP includes planarizing the cap layer and the interconnect layer between a rotatable polishing head and a rotatable polishing platen at a planarizing pressure ranging of at least 5.0 psi.

18. The method of Claim 1 wherein the device is a split gate field effect transistor.

19. A semiconductor device, comprising:

a source region formed in a substrate;

a gate oxide layer formed over the substrate and having an opening over the source region;

a gate layer formed over the gate oxide and having an opening exposing the source region and defining split gates opposing the source region;

a source interconnect formed over the source region;

spacers formed over and beside the split gates to isolate the split gates from the source interconnect;

isolation layers formed on the substrate and on outside walls of the spacers; and

line interconnects formed laterally adjacent the spacers and over the isolation layers;

wherein the spacers, isolation layers and line interconnects collectively form a substantially planar surface.

20. A method of planarizing topographic features on a substrate, comprising:

providing a substrate having a plurality of layers formed thereon, the layers forming a plurality of topographic features of varying heights relative to a reference plane that is parallel to a principal plane of the substrate;

coupling the substrate to a rotatable polishing head;

contacting the topographic features with a rotatable polishing platen; and

maintaining the contacting while rotating at least one of the polishing head and the polishing platen, thereby removing portions of the topographic features to form a substantially planar surface.

21. The method of Claim 20 wherein rotating includes rotating the polishing head at a speed ranging between 75 rpm and 200 rpm.

22. The method of Claim 21 wherein the contacting is done at a pressure of at least 5.0 psi .

23. The method of Claim 20 wherein rotating includes rotating the polishing platen at a speed ranging between 65 rpm and 150 rpm.

24. The method of Claim 23 wherein the speed is 87 rpm.

25. The method of Claim 20 wherein the plurality of layers includes an interconnect layer formed over a semiconductor device gate structure and a cap layer formed over the interconnect layer, wherein portions of the interconnect layer are removed at a slower rate than portions of the cap layer are removed.

25. A method of forming a box-shaped interconnect, comprising:

forming an interconnect layer above and beside an electrode structure;

forming a cap layer over the interconnect layer;

planarizing the cap layer and interconnect layer to leave an exposed portion of the interconnect layer and a capped portion of the interconnect layer;

forming a hard mask over the exposed portion of the interconnect layer; and

removing the capped portion of the interconnect layer.

26. The method of claim 25 wherein the electrode structure is a split gate.